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FIG. 1

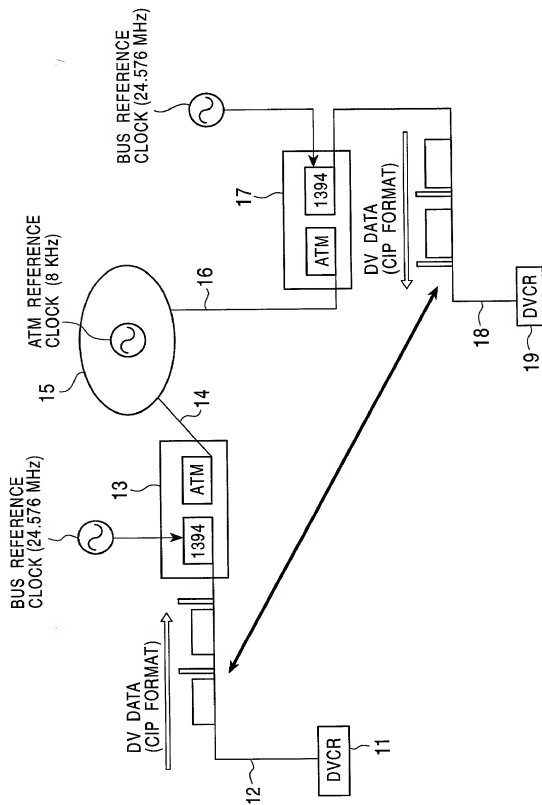
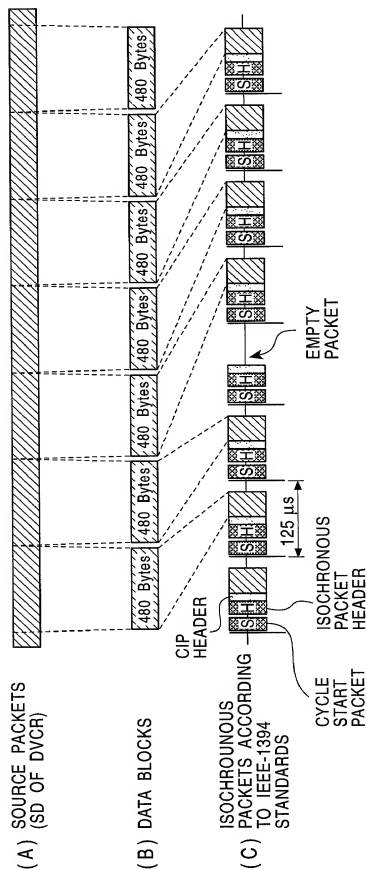


FIG. 2



The diagram illustrates the timing relationship between an NTSC video frame and an IEEE-1394 bus cycle. It consists of four horizontal timelines labeled (A) through (D).

- (A) NTSC FRAME TIMING SAMPLED AT 24.576 MHz AT A SENDER END:** Shows a timeline with vertical tick marks every 1/24.576 μs. Key time points are labeled t1, t3, t4, t6, t7, t8, t9. Intervals are marked: "ADDED TIME" (from t1 to t3), "DELAY" (from t3 to t4), and "TdelayAdd" (from t4 to t6).
- (B) IEEE-1394 BUS CYCLE (125 μs):** Shows a timeline with vertical tick marks every 1/125 μs. Key time points are labeled t12, t5, t11. It includes two rectangular pulses labeled CIP₁ and CIP₂. Arrows indicate the "INSERTION OF TIME STAMP" at t12 and the "EXTRACTION OF TIME STAMP" at t5.
- (C) IEEE-1394 BUS CYCLE (125 μs):** Similar to (B), it shows the bus cycle with CIP₁ and CIP₂ pulses. Arrows indicate the "EXTRACTION OF TIME STAMP" at t11 and the "INSERTION OF TIME STAMP" at t5.
- (D) NTSC FRAME TIMING SAMPLED AT 24.576 MHz AT A RECEIVER END:** Shows a timeline with vertical tick marks every 1/24.576 μs. Key time points are labeled t1, t3, t4, t6, t7, t8, t9. Intervals are marked: "ADDED TIME" (from t1 to t3), "DELAY" (from t3 to t4), and "TdelayAdd" (from t4 to t6).

Horizontal dashed lines connect corresponding time points across the timelines: t1 to t1, t3 to t3, t4 to t4, t6 to t6, t7 to t7, t8 to t8, and t9 to t9. A double-headed arrow at the bottom indicates a 29.97 Hz frequency difference between the sender and receiver timelines.

(D) NTSC FRAME TIMING
SAMPLED AT 24.576 MHZ
AT A RECEIVER END

FIG. 4

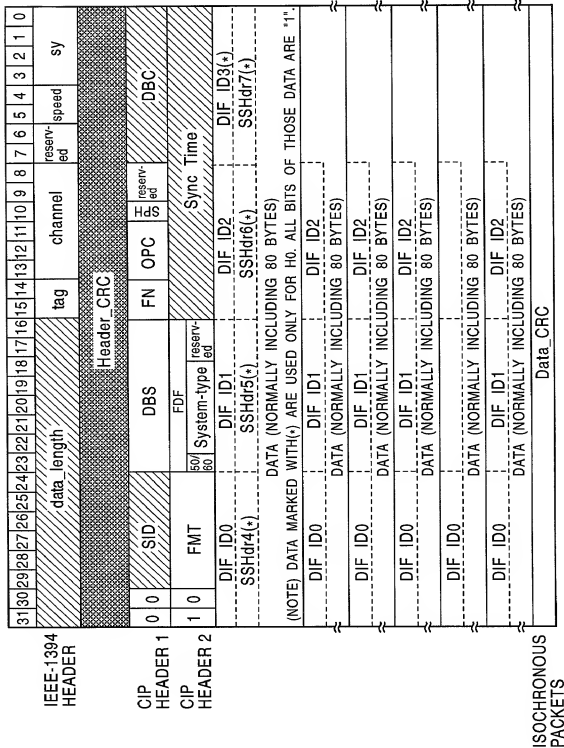


FIG. 5

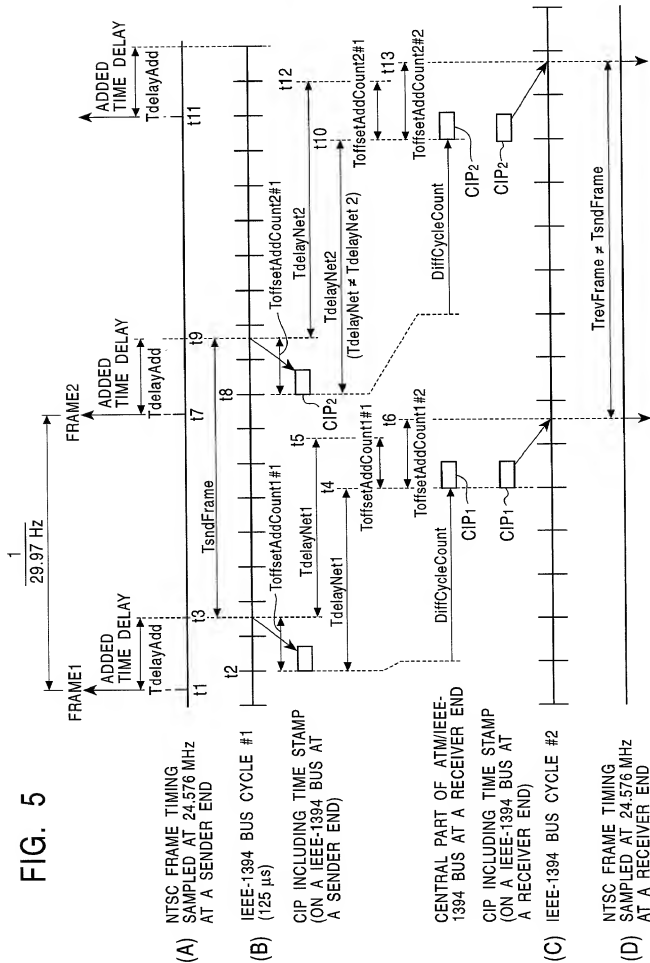


FIG. 6

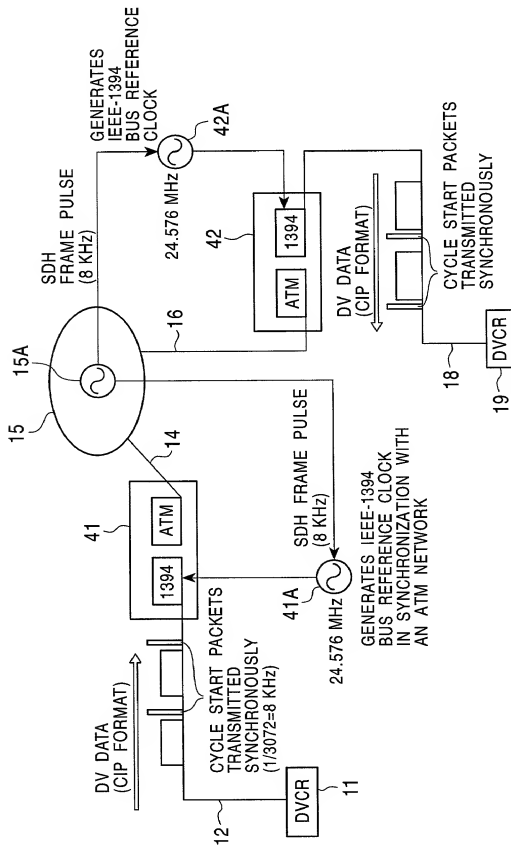


FIG. 7

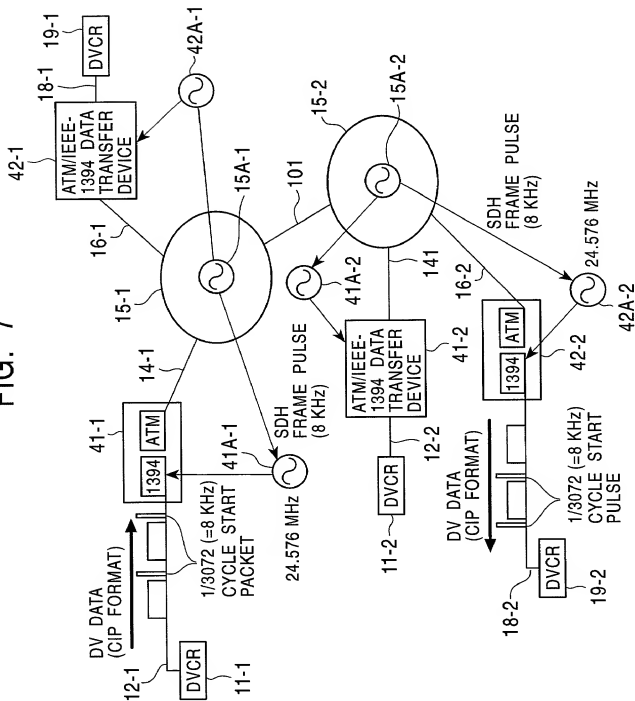


FIG. 8

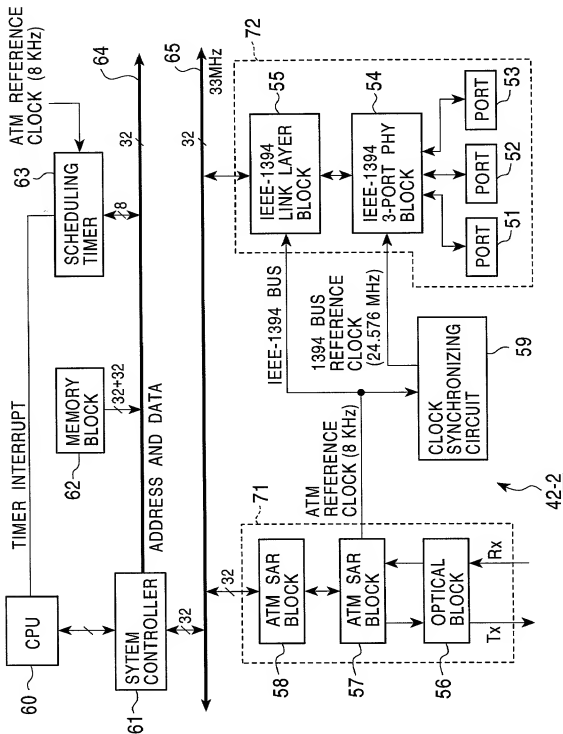
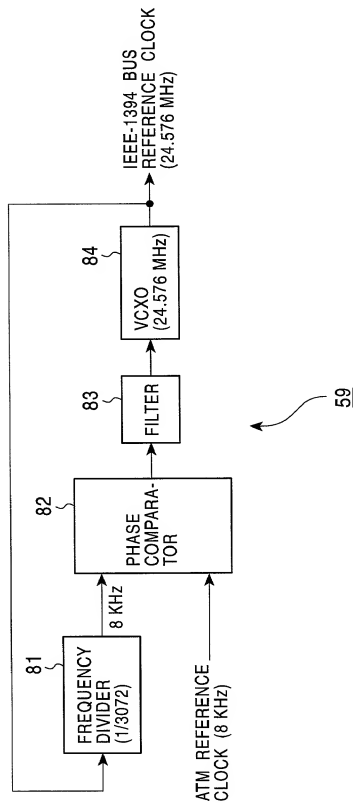


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FIG. 10

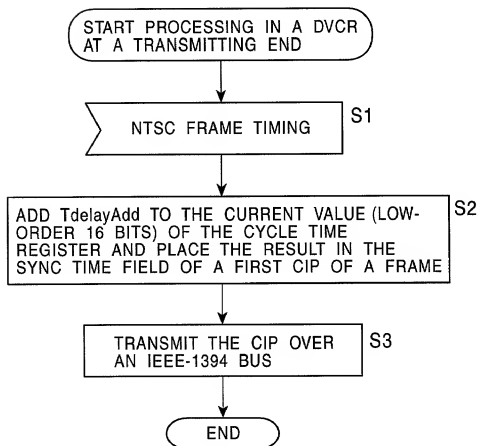


FIG. 11

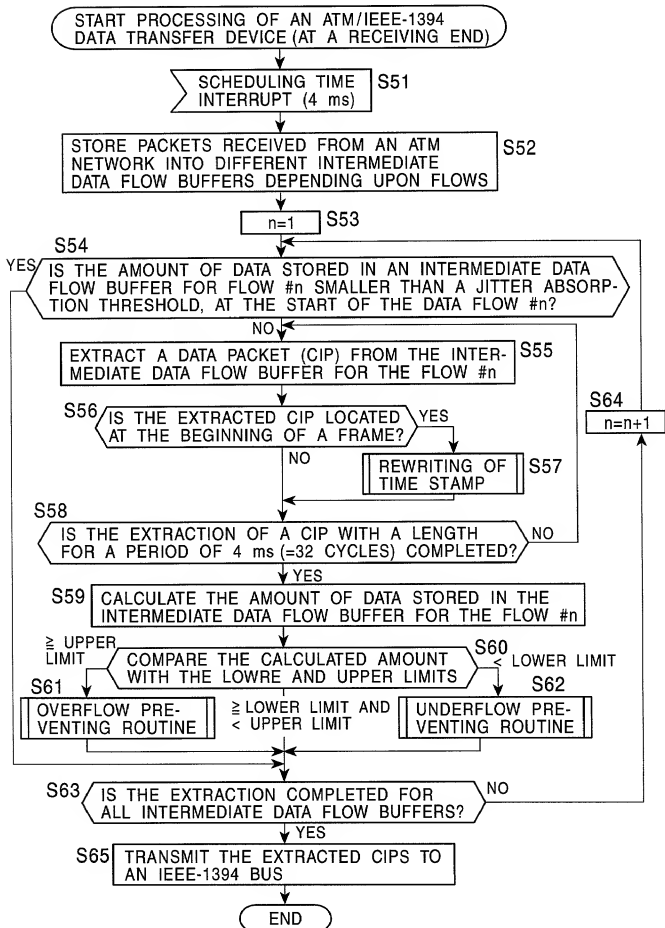


FIG. 12

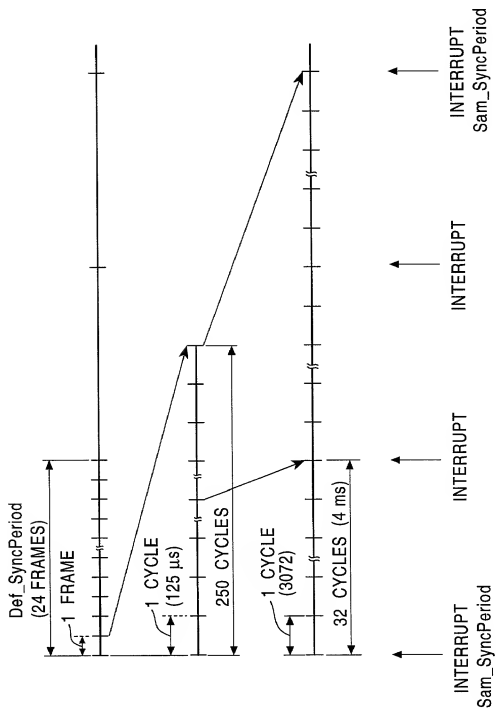


FIG. 13

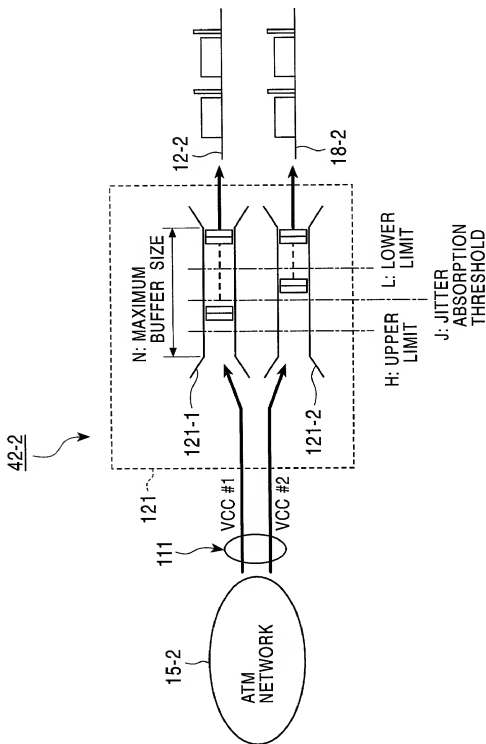
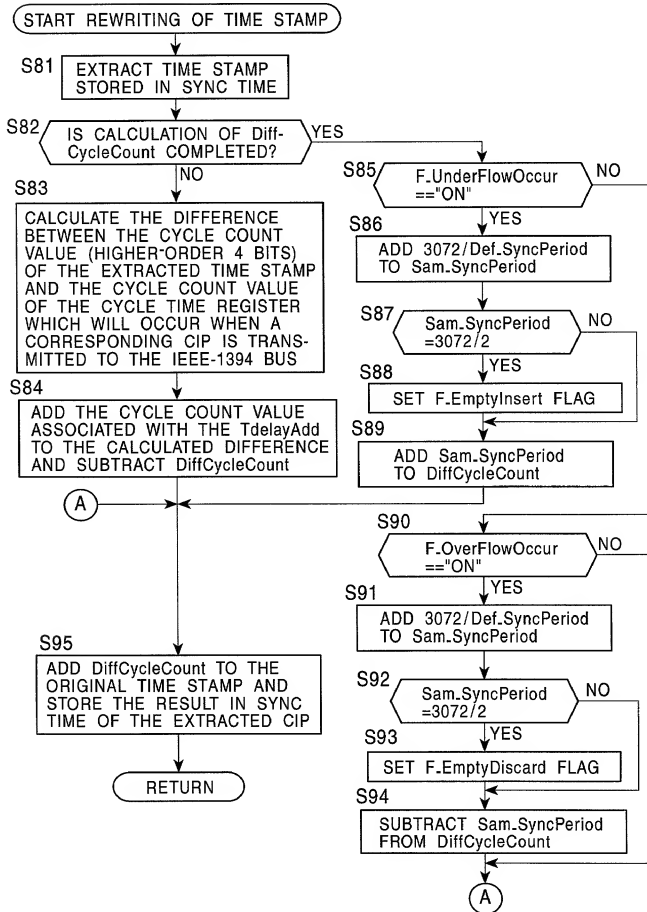
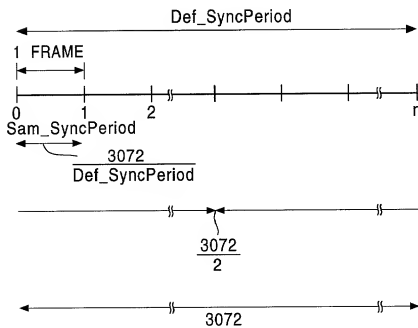


FIG. 14



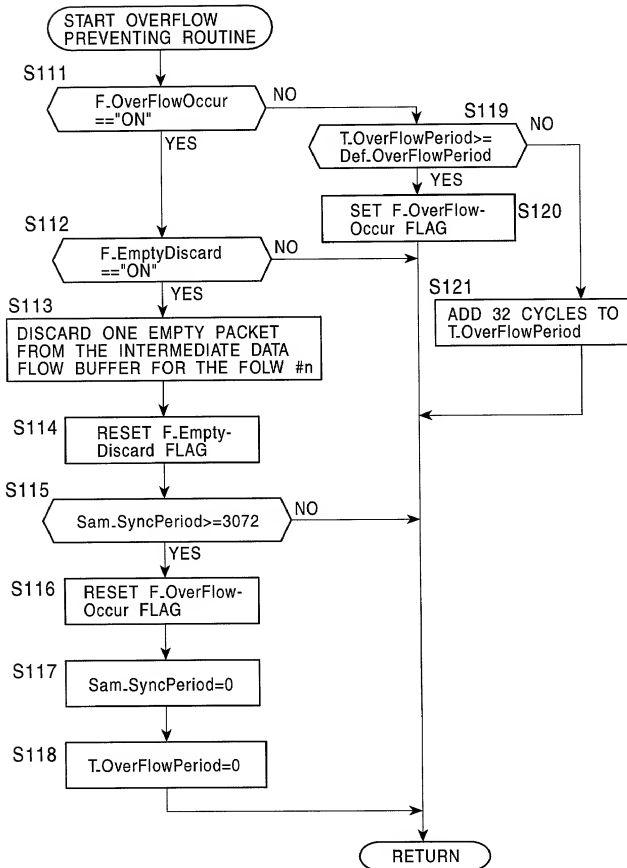
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FIG. 15



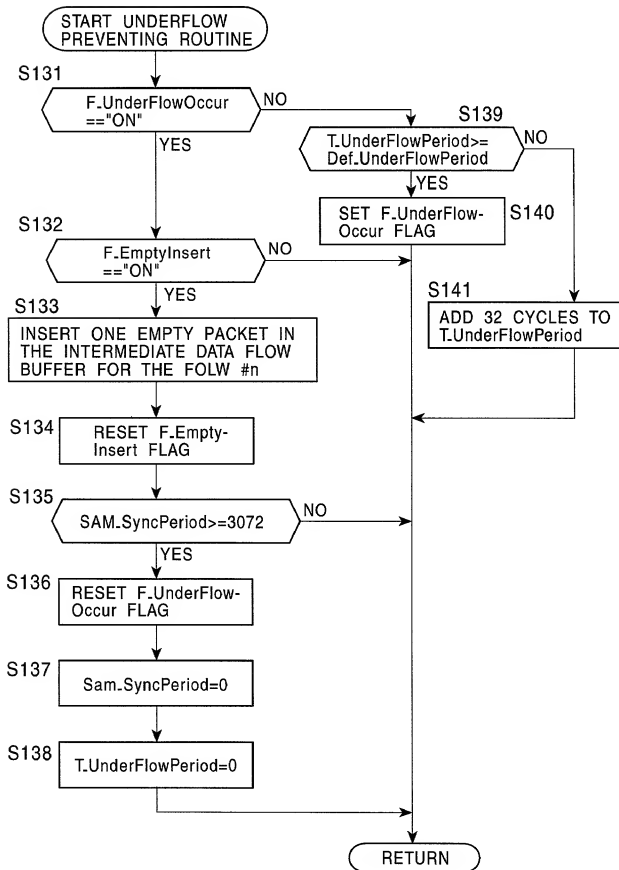
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FIG. 16



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FIG. 17



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FIG. 18

